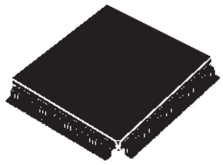
ST70135A

ASCOT^{TM} DMT TRANSCEIVER

- DMT MODEM FOR CPE ADSL, COMPATIBLE WITH THE FOLLOWING STANDARDS:
  - ANSI T1.413 ISSUE 2
  - ITU-T G.992.1 (G.DMT)
  - ITU-T G.992.2 (G.LITE)
- SUPPORTS EITHER ATM (UTOPIA LEVEL 1 & 2) OR BITSTREAM INTERFACE
- 16 BIT MULTIPLEXED MICROPROCESSOR INTERFACE (LITTLE AND BIG ENDIAN COMPATIBILITY)
- ANALOG FRONT END MANAGEMENT
- DUAL LATENCY PATHS: FAST AND INTERLEAVED
- ATM'S PHY LAYER: CELL PROCESSING (CELL DELINEATION, CELL INSERTION, HEC)
- ADSL'S OVERHEAD MANAGEMENT
- REED SOLOMON ENCODE/DECODE
- TRELLIS ENCODE/DECODE (VITERBI)
- DMT MAPPING/ DEMAPPING OVER 256 CARRIERS
- FINE (2PPM) TIMING RECOVER USING ROTOR AND ADAPTATIVE FREQUENCY DOMAIN EQUALIZING
- TIME DOMAIN EQUALIZATION
- FRONT END DIGITAL FILTERS
- 0.35µm HCMOS6 TECHNOLOGY
- 144 PIN PQFP PACKAGE
- POWER CONSUMPTION 1 WATT AT 3.3V



PQFP144
ORDERING NUMBER:
ST70135A

APPLICATIONS

Routers at SOHO, stand-alone modems, PC modems

GENERAL DESCRIPTION

The ST70135A is the DMT modem and ATM framer of the STMicroelectronics ASCOT™ chipset. When coupled with ST70134 analog front-end and an external controller running dedicated firmware, the product fulfills ANSI T1.413 "Issue 2" DMT ADSL specification.

The chip supports UTOPIA level 1 and UTOPIA level 2 interface and a non ATM synchronous bit-stream interface.

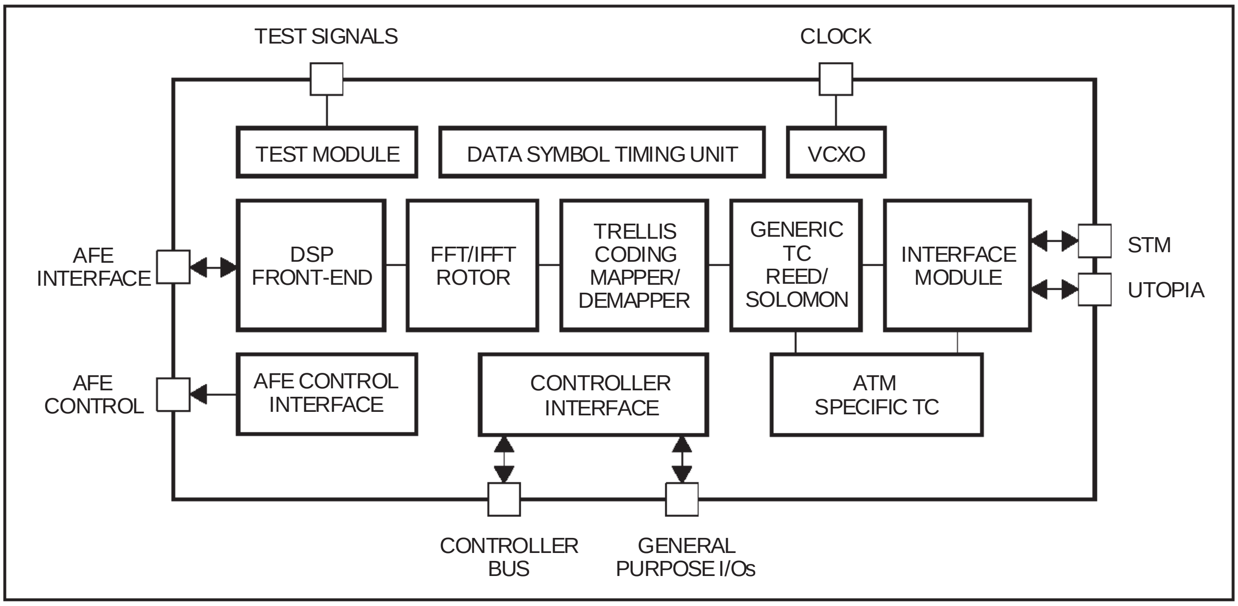
The ST70135A can be split up into two different sections. The physical one performs the DMT modulation, demodulation, Reed-Solomon encoding, bit interleaving and 4D trellis coding.

The ATM section embodies framing functions for the generic and ATM Transmission Convergence (TC) layers.

The generic TC consists of data scrambling and Reed Solomon error corrections, with and without interleaving. The ST70135A is controlled and programmed by an external controller (ADSL Transceiver Controller, ATC) that sets the programmable coefficients.

The firmware controls the initialization phase and carries out the consequent adaptation operations.

Figure 1 : Block Diagram



TRANSIENT ENERGY CAPABILITIES

ESD

ESD (Electronic Discharged) tests have been performed for the Human Body Model (HBM) and for the Charged Device Model (CDM). The pins of the device are to be able to withstand minimum 2000V for the HBM and minimum 250V for CDM.

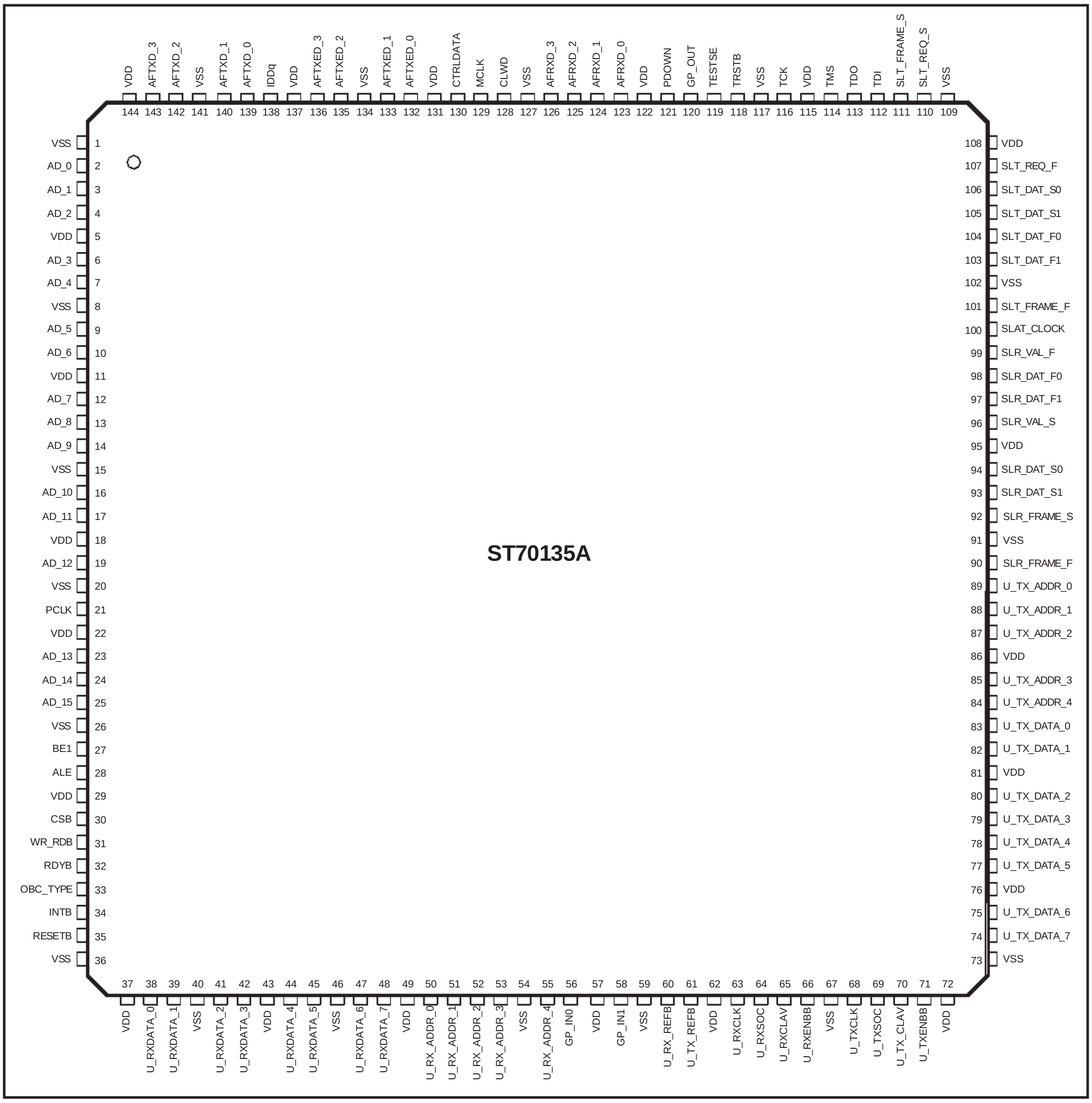
Latch-up

The maximum sink or source current from any pin is limited to 200mA to prevent latch-up.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
P_{tot}	Total Power Dissipation		900	1400	mW
T_{amb}	Ambient Temperature 1m/s airflow	0		70	°C

Figure 2 : Pin Connection



PIN FUNCTIONS

Pin	Name	Type	Supply	Driver	BS	Function
1	VSS			0V Ground		
2	AD_0	B	VDD	BD8SCR	B	Data 0
3	AD_1	B	VDD	BD8SCR	B	Data 1
4	AD_2	B	VDD	BD8SCR	B	Address / Data 2
5	VDD					(VSS + 3.3V) Power Supply
6	AD_3	B	VDD	BD8SCR	B	Address / Data 3
7	AD_4	B	VDD	BD8SCR	B	Address / Data 4
8	VSS					0V Ground
9	AD_5	B	VDD	BD8SCR	B	Address / Data 5
10	AD_6	B	VDD	BD8SCR	B	Address / Data 6
11	VDD					(VSS + 3.3V) Power Supply
12	AD_7	B	VDD	BD8SCR	B	Address / Data 7
13	AD_8	B	VDD	BD8SCR	B	Address / Data 8
14	AD_9	B	VDD	BD8SCR	B	Address / Data 9
15	VSS					0V Ground
16	AD_10	B	VDD	BD8SCR	B	Address / Data 10
17	AD_11	B	VDD	BD8SCR	B	Address / Data 11
18	VDD					(VSS + 3.3V) Power Supply
19	AD_12	B	VDD	BD8SCR	B	Address / Data 12
20	VSS					0V Ground
21	PCLK	I	VDD	IBUF	I	Processor clock
22	VDD					(VSS + 3.3V) Power Supply
23	AD_13	B	VDD	BD8SCR	B	Address / Data 13
24	AD_14	B	VDD	BD8SCR	B	Address / Data 14
25	AD_15	B	VDD	BD8SCR	B	Address / Data 15
26	VSS					0V Ground
27	BE1	I	VDD	IBUF	I	Address 1
28	ALE	I	VDD	IBUF	C	Address Latch
29	VDD					(VSS + 3.3V) Power Supply
30	CSB	I	VDD	IBUF	I	Chip Select
31	WR_RDB	I	VDD	IBUF	I	Specifies the direction of the access cycle
32	RDYB	OZ	VDD	BT4CR	O	Controls the ATC bus cycle termination
33	OBC_TYPE	I-PD	VDD	IBUF	I	ATC Mode Selection (0 = i960; 1 = generic)
34	INTB	O	VDD	IBUF	O	Requests ATC interrupt service
35	RESETB	I	VDD	IBUF	I	Hard reset
36	VSS					0V Ground

PIN FUNCTIONS (continued)

Pin	Name	Type	Supply	Driver	BS	Function
37	VDD					(VSS + 3.3V) Power Supply
38	U_RxData_0	OZ	VDD	BD8SRC	B	Utopia RX Data 0
39	U_RxData_1	OZ	VDD	BD8SRC	B	Utopia RX Data 1
40	VSS					0V Ground
41	U_RxData_2	OZ	VDD	BD8SRC	B	Utopia RX Data 2
42	U_RxData_3	OZ	VDD	BD8SRC	B	Utopia RX Data 3
43	VDD					(VSS + 3.3V) Power Supply
44	U_RxData_4	OZ	VDD	BD8SRC	B	Utopia RX Data 4
45	U_RxData_5	OZ	VDD	BD8SRC	B	Utopia RX Data 5
46	VSS					0V Ground
47	U_RxData_6	OZ	VDD	BD8SRC	B	Utopia RX Data 6
48	U_RxData_7	OZ	VDD	BD8SRC	B	Utopia RX Data 7
49	VDD					(VSS + 3.3V) Power Supply
50	U_RxADDR_0	I	VDD	IBUF	I	Utopia RX Address 0
51	U_RxADDR_1	I	VDD	IBUF	I	Utopia RX Address 1
52	U_RxADDR_2	I	VDD	IBUF	I	Utopia RX Address 2
53	U_RxADDR_3	I	VDD	IBUF	I	Utopia RX Address 3
54	VSS					0V Ground
55	U_RxADDR_4	I	VDD	IBUF	I	Utopia RX Address 4
56	GP_IN_0	I-PD	VDD	IBUFDQ	I	General purpose input 0
57	VDD					(VSS + 3.3V) Power Supply
58	GP_IN_1	I-PD	VDD	IBUFDQ	I	General purpose input 1
59	VSS					0V Ground
60	U_RxRefB	O	VDD	IBUF	O	8kHz clock to ATM device
61	U_TxRefB	I	VDD	BT4CR	I	8kHz clock from ATM device
62	VDD					(VSS + 3.3V) Power Supply
63	U_Rx_CLK	I	VDD	IBUF		Utopia RX Clock
64	U_Rx_SOC	OZ	VDD	BD8SCR		Utopia RX Start of Cell
65	U_RxCLAV	OZ	VDD	BD8SCR		Utopia RX Cell Available
66	U_RxENBB	I	VDD	IBUF		Utopia RX Enable
67	VSS					0V Ground
68	U_Tx_CLK	I	VDD	IBUF		Utopia TX Clock
69	U_Tx_SOC	I	VDD	IBUF		Utopia TX Start of Cell
70	U_TxCLAV	OZ	VDD	BD8SCR		Utopia TX Cell Available
71	U_TxENBB	I	VDD	IBUF		Utopia TX Enable
72	VDD					(VSS + 3.3V) Power Supply

PIN FUNCTIONS (continued)

Pin	Name	Type	Supply	Driver	BS	Function
73	VSS					0V Ground
74	U_TxData_7	I	VDD	IBUF	I	Utopia TX Data 7
75	U_TxData_6	I	VDD	IBUF	I	Utopia TX Data 6
76	VDD					(VSS + 3.3V) Power Supply
77	U_TxData_5	I	VDD	IBUF	I	Utopia TX Data 5
78	U_TxData_4	I	VDD	IBUF	I	Utopia TX Data 4
79	U_TxData_3	I	VDD	IBUF	I	Utopia TX Data 3
80	U_TxData_2	I	VDD	IBUF	I	Utopia TX Data 2
81	VDD					(VSS + 3.3V) Power Supply
82	U_TxData_1	I	VDD	IBUF	I	Utopia TX Data 1
83	U_TxData_0	I	VDD	IBUF	I	Utopia TX Data 0
84	U_TxADDR_4	I	VDD	IBUF	I	Utopia TX Address 4
85	U_TxADDR_3	I	VDD	IBUF	I	Utopia TX Address 3
86	VDD					(VSS + 3.3V) Power Supply
87	U_TxADDR_2	I	VDD	IBUF	I	Utopia TX Address 2
88	U_TxADDR_1	I	VDD	IBUF	I	Utopia TX Address 1
89	U_TxADDR_0	I	VDD	IBUF	I	Utopia TX Address 0
90	SLR_ FRAME_F	O	VDD	BT4CR		Frame Identifier Fast
91	VSS					0V Ground
92	SLR_FRAME_S	O	VDD	BT4CR		Receive Frame Identifier Interleaved
93	SLR_DATA_S_1	O	VDD	BT4CR		Receive Data Interleave 1
94	SLR_DATA_S_0	O	VDD	BT4CR		Receive Data Interleave 0
95	VDD					(VSS + 3.3V) Power Supply
96	SLR_VAL_S	O	VDD	BT4CR		Receive Data Valid Indicator Interleaved
97	SLR_DATA_F_1	O	VDD	BT4CR		Receive Data Fast 1
98	SLR_DATA_F_0	O	VDD	BT4CR		Receive Data Fast 0
99	SLR_VAL_F	O	VDD	BT4CR		Receive Data Valid Indicator Fast
100	SLAP_CLOCK	O	VDD	BT4CR		Clock for SLAP I/F
101	SLT_FRAME_F	O	VDD	BT4CR		Transmit Start of frame Indicator Fast
102	VSS					0V Ground
103	SLT_DATA_F_1	I	VDD	IBUFDQ		Transmit Data Fast 1
104	SLT_DATA_F_0	I	VDD	IBUFDQ		Transmit Data Fast 0
105	SLT_DATA_S_1	I	VDD	IBUFDQ		Transmit Data Interleave 1
106	SLT_DATA_S_0	I	VDD	IBUFDQ		Transmit Data Interleave 0
107	SLT_REQ_F	O	VDD	BT4CR		Transmit Byte Request Fast
108	VDD					(VSS + 3.3V) Power Supply

PIN FUNCTIONS (continued)

Pin	Name	Type	Supply	Driver	BS	Function
109	VSS					0V Ground
110	SLT_REQ_S	O	VDD	BT4CR		Transmit Byte Request Interleaved
111	STL_FRAME_S	O	VDD	BT4CR		Transmit Start of frame Indication Interleaved
112	TDI	I-PU	VDD	IBUFUQ		JTAG I/P
113	TDO	OZ	VDD	BT4CR		JTAG O/P
114	TMS	I-PU	VDD	IBUFUQ		JTAG Made Select
115	VDD					(VSS + 3.3V) Power Supply
116	TCK	I-PD	VDD	IBUFDQ		JTAG Clock
117	VSS					0V Ground
118	TRSTB	I-PD	VDD	IBUFDQ		JTAG Reset
119	TESTSE	I	VDD	IBUF	none	Enables scan test mode
120	GP_OUT	O	VDD	BD8SCR	O	General purpose output
121	PDOWN	O	VDD	BT4CR	O	Power down analog front end (Reset)
122	VDD					(VSS + 3.3V) Power Supply
123	AFRXD_0	I	VDD	IBUF	I	Receive data nibble
124	AFRXD_1	I	VDD	IBUF	I	Receive data nibble
125	AFRXD_2	I	VDD	IBUF	I	Receive data nibble
126	AFRXD_3	I	VDD	IBUF	I	Receive data nibble
127	VSS					0V Ground
128	CLWD	I	VDD	IBUF	I	Start of word indication
129	MCLK	I	VDD	IBUF	C	Master clock
130	CTRLDATA	O	VDD	BT4CR	O	Serial data Transmit channel
131	VDD					(VSS + 3.3V) Power Supply
132	AFTXED_0	O	VDD	BT4CR	O	Transmit echo nibble
133	AFTXED_1	O	VDD	BT4CR	O	Transmit echo nibble
134	VSS					0V Ground
135	AFTXED_2	O	VDD	BT4CR	O	Transmit echo nibble
136	AFTXED_3	O	VDD	BT4CR	O	Transmit echo nibble
137	VDD					(VSS + 3.3V) Power Supply
138	IDDq	I	VDD	IBUF	none	Test pin, active high
139	AFTXD_0	O	VDD	BT4CR	O	Transmit data nibble
140	AFTXD_1	O	VDD	BT4CR	O	Transmit data nibble
141	VSS					0V Ground
142	AFTXD_2	O	VDD	BT4CR	O	Transmit data nibble
143	AFTXD_3	O	VDD	BT4CR	O	Transmit data nibble
144	VDD					(VSS + 3.3V) Power Supply

I/O DRIVER FUNCTION

Driver	Function
BD4CR	CMOS bidirectional, 4mA, slew rate control
BD8SCR	CMOS bidirectional, 8mA, slew rate control, Schmitt trigger
IBUF	CMOS input
IBUFDQ	CMOS input, pull down, IDDq control
IBUFUQ	CMOS input, pull up, IDDq control

PIN SUMMARY

Mnemonic	Type	BS Type	Signals	Function
Power Supply				
VDD				(VSS + 3.3V) Power Supply
VSS				0V Ground
ATC INTERFACE				
ALE	I	C	1	Used to latch the address of the internal register to be accessed
PCLK	I	I	1	Processor clock
CSB	I	I	1	Chip selected to respond to bus cycle
BE1	I	I	1	Address 1 (not multiplexed)
WR_RDB	I	I	1	Specifies the direction of the access cycle
RDYB	OZ	O	1	Controls the ATC bus cycle termination
INTB	O	O	1	Requests ATC interrupt service
AD	IO	B	16	Multiplexed Address/Data bus
OBC_TYPE	I-PD	I	1	Select between i960 (0) or generic (1) controller interface
TEST ACCESS PART INTERFACE				
TDI	I-PU		1	Refer to section
TDO	OZ		1	
TCK	I-PD		1	
TMS	I-PU		1	
TRSTB	I-PD		1	
ANALOG FRONT END INTERFACE				
AFRXD	I	I	4	Receive data nibble
AFTXD	O	O	4	Transmit data nibble
AFTXED	O	O	4	Transmit echo nibble
CLWD	I	I	1	Start of word indication
PDOWN	O	O	1	Power down analog front end
CTRLDATA	O	O	1	Serial data transmit channel
MCLK	I	C	1	Master cloc

Mnemonic	Type	BS Type	Signals	Function
ATM UTOPIA INTERFACE				
U_RxData	OZ	B	8	Receive interface Data
U_TxData	I	I	8	Transmit interface Data
U_RxADDR	I	I	5	Receive interface Address
U_TxADDR	I	I	5	Transmit interface Address
U_RxCLAV	OZ	O	1	Receive interface Cell Available
U_TxCLAV	OZ	O	1	Transmit interface Cell Available
U_RxENBB	I-TTL	I	1	Receive interface Enable
U_TxENBB	I-TTL	I	1	Transmit interface Enable
U_RxSOC	OZ	O	1	Receive interface Start of Cell
U_TxSOC	I-TTL	I	1	Transmit interface Start of Cell
U_RxCLK	I-TTL	C	1	Receive interface Utopia Clock
U_TxCLK	I-TTL	C	1	Transmit interface Utopia Clock
U_RxRefB	O	O	1	8kHz reference clock to ATM device
U_TxRefB	I-TTL	I	1	8kHz reference clock from ATM device
ATM SLAP INTERFACE				
SLR_VAL_S	O		1	
SLR_VAL_F	O		1	
SLR_DATA_S	O		2	
SLR_DATA_F	O		2	
SLT_REQ_S	O		1	
SLT_REQ_F	O		1	
SLT_DATA_S	I		2	
SLT_DATA_F	I		2	
SLAP_CLOCK	O		1	
SLR_FRAME_I	O		1	
SLT_FRAME_I	O		1	
SLR_FRAME_F	O		1	
SLT_FRAME_F	O		1	
MISCELLANEOUS				
GP_IN	I-PD	I	2	General purpose input
GP_OUT	O	O	1	General purpose output
RESETB	I	I	I	Hard reset
TESTSE	I	none	none	Enable scan test mode
IDDq	I	none	none	Test pin, active high

I	=	Input, CMOS levels
I-PU	=	Input with pull-up resistance, CMOS levels
I-PD	=	Input with pull-down resistance, CMOS levels
I-TTL	=	Input TTL levels
O	=	Push-pull output
OZ	=	Push-pull output with high-impedance state
IO	=	Input / Tristate Push-pull output
BS cell	=	Boundary-Scan cell
I	=	Input cell
O	=	Output cell
B	=	Bidirectional cell
C	=	Clock

Main Block Description

The following drawings describe the sequence of functions performed by the chip.

DSP Front-End

The DSP Front-End contains 4 parts in the receive direction: the Input Selector, the Analog Front-End Interface, the Decimator and the Time Equalizer. The input selector is used internally to enable test loopbacks inside the chip. The Analog Front-End Interface transfers 16-bit words, multiplexed on 4 input/output signals. Word transfer is carried out in 4 clock cycles.

The Decimator receives 16-bit samples at 8.8MHz (as sent by the Analog Front-End chip: ST70134) and reduces this rate to 2.2MHz.

The Time Equalizer (TEQ) module is a FIR filter with programmable coefficients. Its main purpose is to reduce the effect of Inter-Symbol Interferences (ISI) by shortening the channel impulse response. Both the Decimator and TEQ can be bypassed. In the transmit direction, the DSP Front-End includes: sidelobe filtering, clipping, delay equalization and interpolation. The sidelobe filtering and delay equalization are implemented by IIR Filters, reducing the effect of echo in FDM systems. Clipping is a statistical process limiting the amplitude of the output signal, optimizing the dynamic range of the AFE. The interpolator receives data at 2.2MHz and generates samples at a rate of 8.8MHz.

DMT Modem

This module is a programmable DSP unit. Its instruction set enables the basic functions of the DMT algorithm like FFT, IFFT, Scaling, Rotor and Frequency Equalization (FEQ) in compliance with ANSI T1.413 specifications.

In the RX path, the 512-point FFT transforms the time-domain DMT symbol into a frequency domain representation which can be further decoded by the subsequent demapping stages.

In other words, the Fast Fourier Transform process is used to transform from time domain to frequency domain (receive path). 1024 time samples are processed. After the first stage time domain equalization and FFT block an ICI (InterCarrier Interference) free information stream turns out.

Figure 3 : DSP Front-End Receive

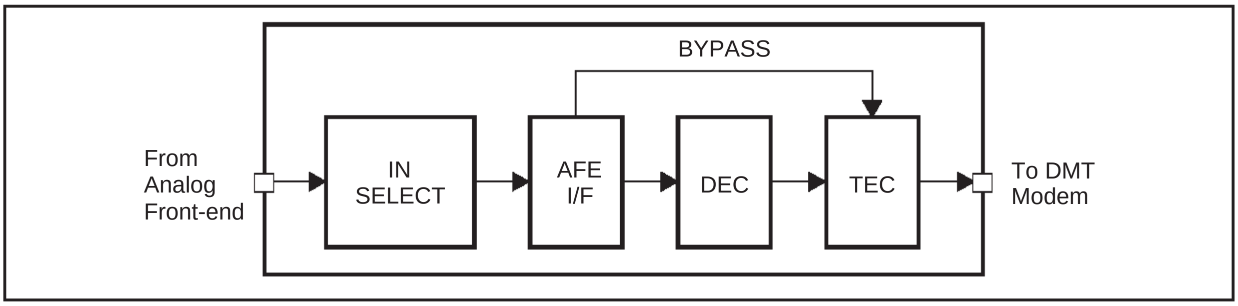


Figure 4 : DSP Front-End Transmit

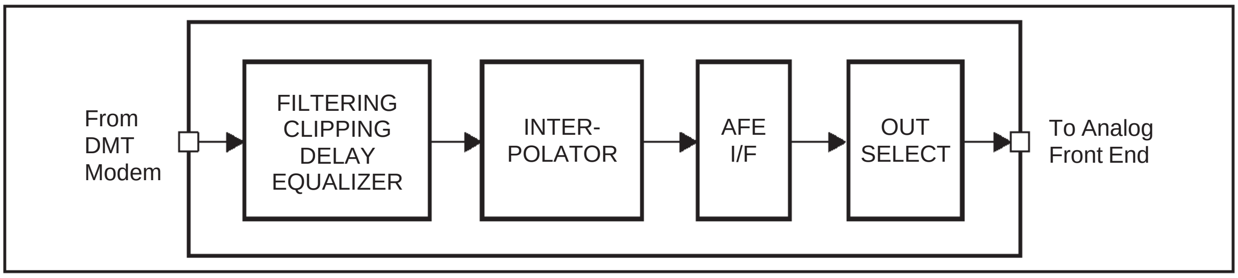
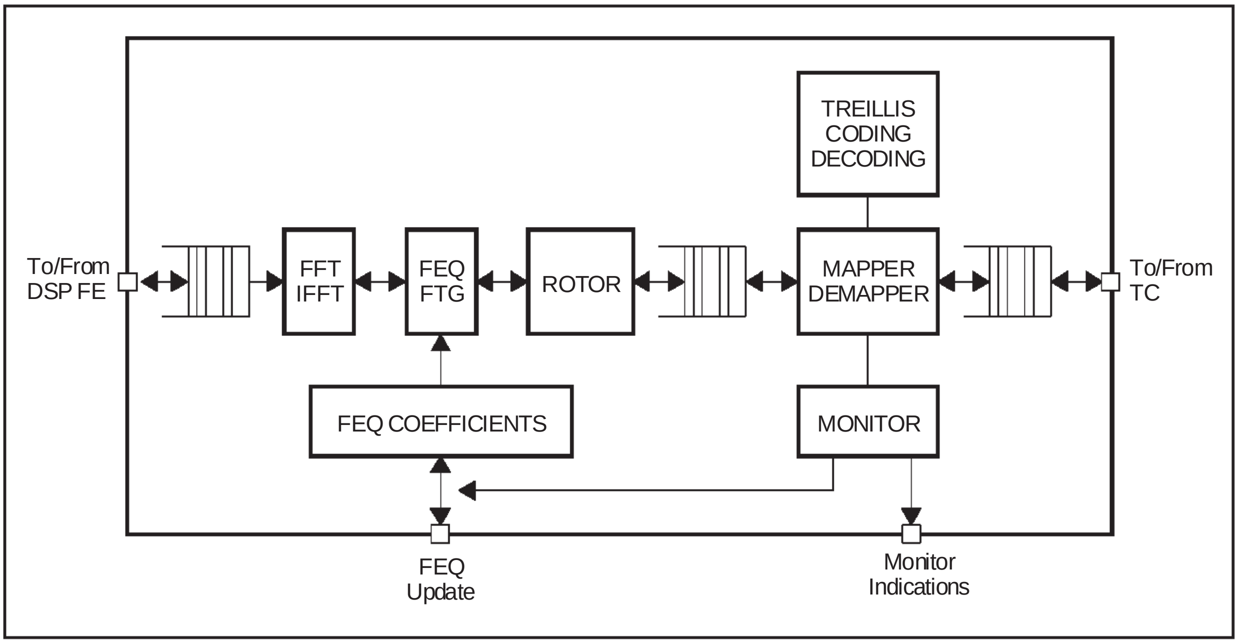


Figure 5 : DMT Modem (Rx & Tx)



This stream is still affected by carrier specific channel distortion resulting in an attenuation of the signal amplitude and a rotation of the signal phase. To compensate, a Frequency domain equalizer (FEQ) and a Rotor (phase shifter) are implemented. The frequency domain equalization performs an operation on the received vector in order to match it with the associated point in the constellation. The coefficient used to perform the equalization are floating point, and may be updated by hardware or software, using a mechanism of active and inactive table to avoid DMT synchro problems.In the transmit path, the IFFT reverses the DMT symbol from frequency domain to time domain.

The IFFT block is preceded by Fine Tune Gain (FTG) and Rotor stages, allowing for a compensation of the possible frequency mismatch between the master clock frequency and the transmitter clock frequency (which may be locked to another reference).

The Inverse Fast Fourier Transform process is used to transform from frequency domain to time domain (transmit path). 256 positive frequencies are processed, giving 512 samples in the time domain.

The FFT module is a slave DSP engine controlled by the firmware running on an external controller. It works off line and communicates with other blocks through buffers controlled by the ”Data Symbol Timing Unit”. The DSP executes a program stored in a RAM area, which constitutes a flexible element that allows for future system enhancements.

DPLL

The Digital PLL module receives a metric for the phase error of the pilot tone. In general, the clock frequencies at the ends (transmitter and receiver) do not match exactly. The phase error is filtered and integrated by a low pass filter, yielding an estimation of the frequency offset. Various processes can use this estimate to deal with the frequency mismatch.

In particular, small accumulated phase error can be compensated in the frequency domain by a rotation of the received code constellation (Rotor). Larger errors are compensated in the time domain by inserting or deleting clock cycles in the sample input sequence.

Eventually that leads to achieve less than 2ppm between the two ends.

Mapper/Demapper, Monitor, Trellis Coding, FEQ Update

The Demapper converts the constellation points computed by the FFT to a block of bits. This means to identify a point in a 2D QAM constellation plane. The Demapper supports Trellis coded demodulation and provides a Viterbi maximum likelihood estimator. When the Trellis is active, the Demapper receives an indication for the most likely constellation subset to be used.

In the transmit direction, the mapper receives a bit stream from the Trellis encoder and modulates the bit stream on a set of carriers (up to 256). It generates coordinates for 2n QAM constellation, where n < 15 for all carriers.

The Mapper performs the inverse operation, mapping a block of bits into one constellation point (in a complex x+jy representation) which is passed to the IFFT block. The Trellis Encoder generates redundant bits to improve the robustness of the transmission, using a 4-Dimensional Trellis Coded Modulation scheme.

This feature can be disabled.The Monitor computes error parameters for carriers specified in the Demapper process.

Those parameters can be used for updates of adaptive filters coefficients, clock phase adjustments, error detection, etc. A series of values is constantly monitored, such as signal power, pilot phase deviations, symbol erasures generation, loss of frame, etc.

Generic TC Layer Functions

These functions relate to byte oriented data streams. They are completely described in ANSI T 1.4 13. Additions described in the Issue 2 of this specification are also supported.

The data received from the demapper may be split into two paths, one dedicated to an interleaved data flow the other one for a fast data flow. No external RAM is needed for the interleaved path.

The interleaving/deinterleaving is used to increase the error correcting capability of block codes for error bursts. After deinterleaving (if applicable), the data flow enters a Reed-Solomon error correcting code decoder, able to correct a number of bytes containing bit errors. The decoder also uses the information of previous receiving stages that may have detected the error bytes and have labelled them with an ”erasure indication”. Each time the RS decoder detects and corrects errors in a RS codeword, an RS correction event is generated.

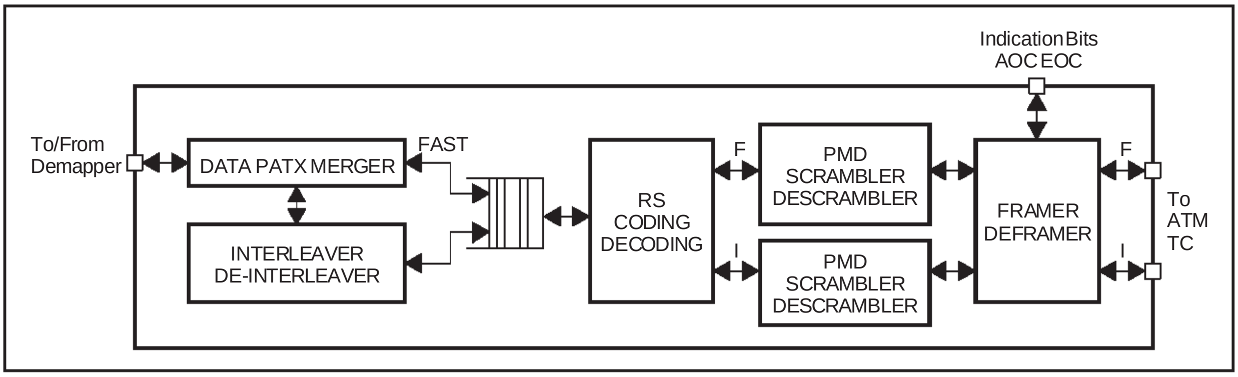
The occurrence of such events can be signalled to the management layer.After the RS decoder, the corrected byte stream is descrambled in the PMD (Physical Medium Dependent) descramblers. Two descramblers are used, for interleaved and non-interleaved data flows.

These are defined in ANSI T1.413. After descrambling, the data flows enter the Deframer that extracts and processes bytes to support Physical layer related functions according to ANSI T1.413. The ADSL frames indeed contain physical layer-related information in addition to the data passed to the higher layers. In particular, the deframer extracts the EOC (Embedded Operations Channel), the AOC (ADSL Overhead Control) and the indicators bits and passes them to the appropriate processing unit (e.g. the transceiver controller).

The deframer also performs a CRC check (Cyclic Redundancy Check) on the received frame and generates events in case of error detection.Event counters can be read by management processes.

The outputs of the deframer are an interleaved and a fast data streams. These data streams can either carry ATM cells or another type of traffic. In the latter case, the ATM specific TC layer functional block, described hereafter, is bypassed and the data stream is directly presented at the input of the interface module.

Figure 6 : Generic TC Layer Functions



ATM Specific TC Layer Functions

The 2 bytes streams (fast and slow) are received from the byte-based processing unit. When ATM cells are transported, this block provides basic cell functions such as cell synchronization, cell payload descrambling, idle/unassigned cell filter, cell Header Error Correction (HEC) and detection.

The cell processing happens according to ITU-T I.163 standard. Provision is also made for BER measurements at this ATM cell level. When non cell oriented byte streams are transported, the cell processing unit is not active.

The interface module collects cells (from the cell-based function module) or a Byte stream (from the deframer). Cells are stored in FIFO's (424 bytes or 8 cell wide, transmit buffers have the same size), from which they are extracted by 2 interface submodules, one providing a Utopia level 1 interface and the other a Utopia level 2 interface.Byte stream are dumped on the SLAP (Synchronous Link Access Protocol) interface. Only one type of interface can be enabled in a specific configuration.

Figure 7 : ATM Specific TC Layer Functions

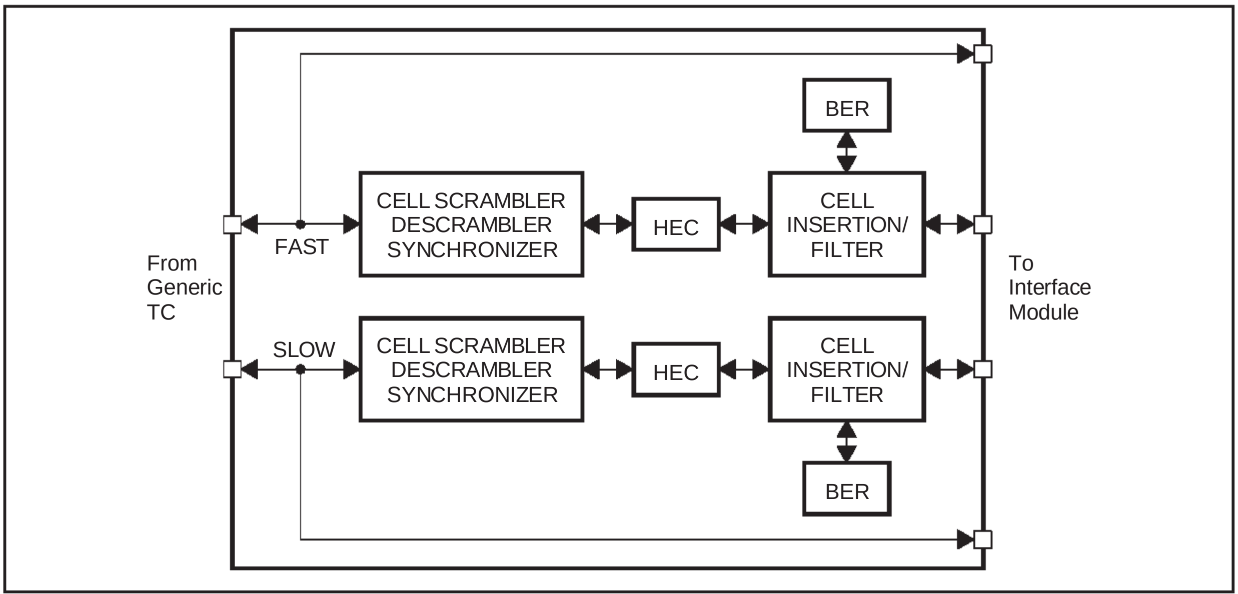
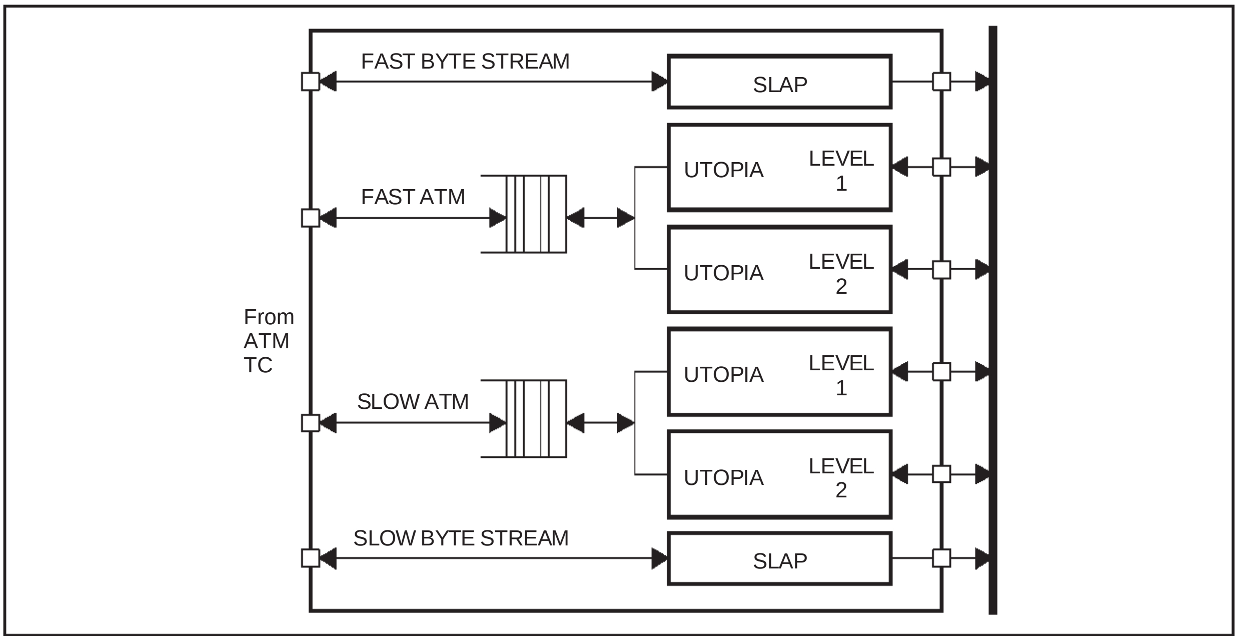


Figure 8 : Interface Module



DMT Symbol Timing Unit (DSTU)

The DSTU interfaces with various modules, like DSP FrontEnd, FFT/IFFT, Mapper/Demapper, RS, Monitor and Transceiver Controller. It consists of a real time and a scheduler modules. The real time unit generates a timebase for the DMT symbols (sample counter), superframes (symbol counter) and hyper-frames (sync counter). The timebases can be modified by various control features. They are continuously fine-tuned by the DPLL module.

The DSTU schedulers execute a program, controlled by program opcodes and a set of variables, the most important of which are real time counters. The transmit and receive sequencers are completely independent and run different programs. An independent set of variables is assigned to each of them. The sequencer programs can be updated in real time.

ST70135A interfaces

Overview

See Figure 9.

Processor Interface (ATC)

The ST70135A is controlled and configured by an external processor across the processor interface. All programmable coefficients and parameters are loaded through this path.

Data and addresses are multiplexed

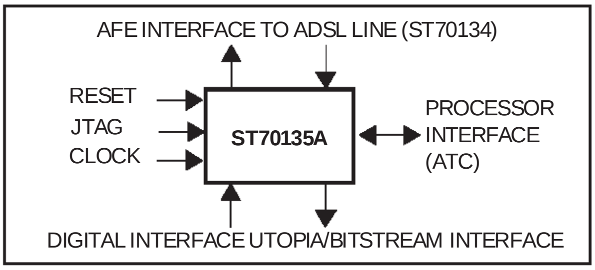
ST70135A works in 16 bits data access, so address bit 0 is not used. Address bit 1 is not multiplexed with data. It has its own pin : BE1.

Byte access are not supported. Access cycle read or write are always in 16 bits data wide, ie bit address A0 is always zero value.

The interrupt request pin to the processor is INTB, and is an Open Drain output.

The ST70135A supports both little and big endian. The default feature is big endian.

Figure 9 : ST70135A Interfaces



Generic Interface

This interface is suitable for a number of processors using a multiplexed Address/data bus. In this case, synchronization of the input signals with PCLK pin is not necessary.

Figure 10 : Generic Processor Interface Write Timing Cycle

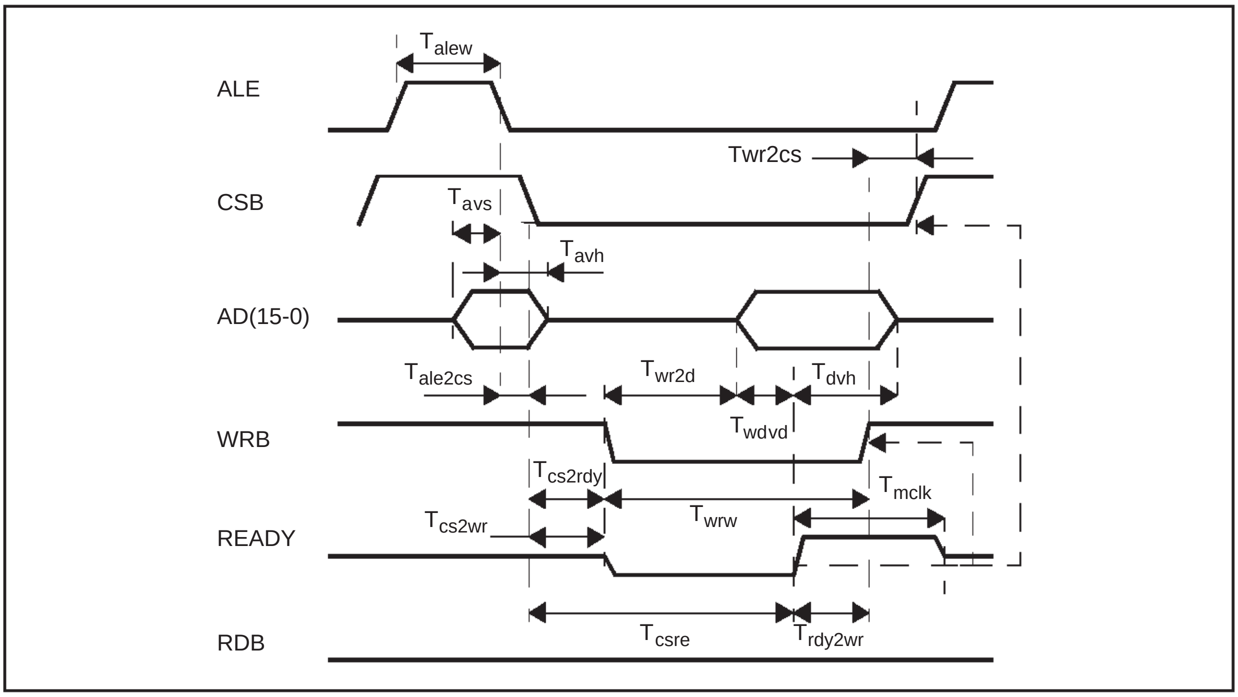
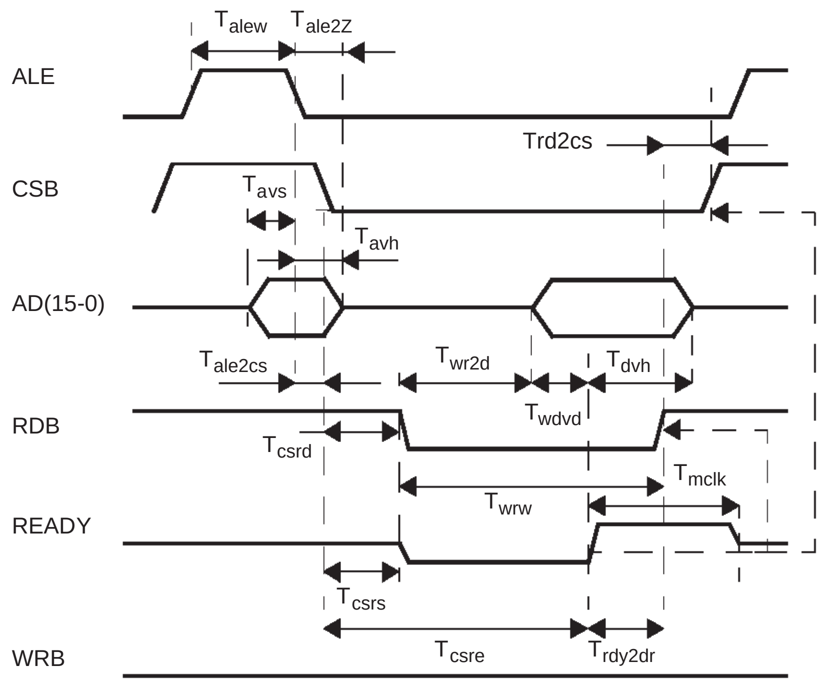


Figure 11 : Generic Processor Interface Read Timing Cycle



Generic processor interface Cycle Timing

All AC characteristics are indicated for a 100pF capacitive load.

Symbol	Parameters	Minimum	Typical	Maximum	Unit
tr & tf	Rise & Fall time (10% to 90%)			3	ns
Talew	ALE pulse width	12			ns
Tavs	Address Valid setup time	10			ns
Tavh	Address Valid Hold time	10			ns
Tale2cs	ALE to CSB	0			ns
Tale2Z	ALE to high Z state of address bus			50	ns
Tcs2rdy	CSB to RDYB asserted			60	ns
Tcsre	Access Time			900	ms
Tcs2wr	CSB to WRB	0			ns
Twr2d	WRB to data			15	ns
Trdy2wr	RDYB to WRB	0			ns
Tdvs	data setup time	10			ns
Tdvh	data hold time	1/2Tmclk		Tmclk	ns
Twr2cs	WRB to CSB	-10			ns
Tcs2rd	CSB to RDB	0			ns
Trdy2rd	RDY to RDB	0			ns
Trd2cs	RDB to CSB	-10			ns
Tmclk	Master clock Timing				

Generic Processor Interface Pins and Functional Description

Name	Type	Function
AD[0..15]	I/O	Multiplexed address / data bus
ALE	I	Address Latch Enable
RDB	I	Read cycle indication
WRB	I	Write cycle indication
CSB	I	Chip Select
RDYB	OZ	Bus cycle ready indication
INTB	O	Interrupt

Digital interface ATM or serial

Digital Interface for data to the loop before modulation and from the loop after demodulation.

This interface collects cells (from the cell based function module) or a byte stream (from the deframer).

Cells are stored in a fifo, 2 interfaces submodules can extract data from the fifo. Byte streams are dumped on the bitstream interface (with no fifo).

3 kinds of interface are allowed:

- Utopia Level 1
- Utopia Level 2
- Bitstream based on a proprietary exchange

The interface selection is programmed by writing the Utopia PHY address register.

Only one interface can be enabled in a ST70135A configuration.

Utopia Level 1 supports only one PHY device. Utopia Level 2 supports multi-PHY devices (See Utopia Level 2 specifications).

Each buffer provides storage for 8 ATM cells (both directions for Fast and Interleaved channel).

The Utopia Level 2 supports point to multipoint configurations by introducing an addressing capability and by making distinction between polling and selecting a device.

Figure 12 : Receive Interface

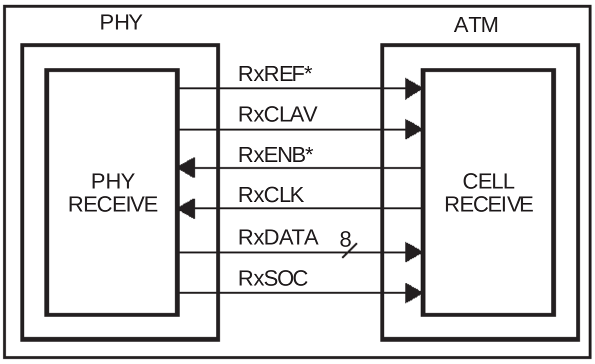
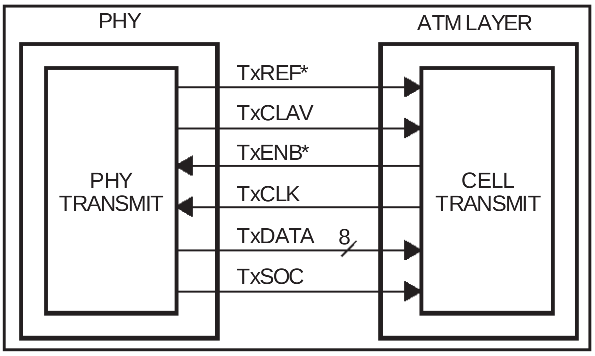


Figure 13 : Transmit Interface



Utopia Level 1 Interface

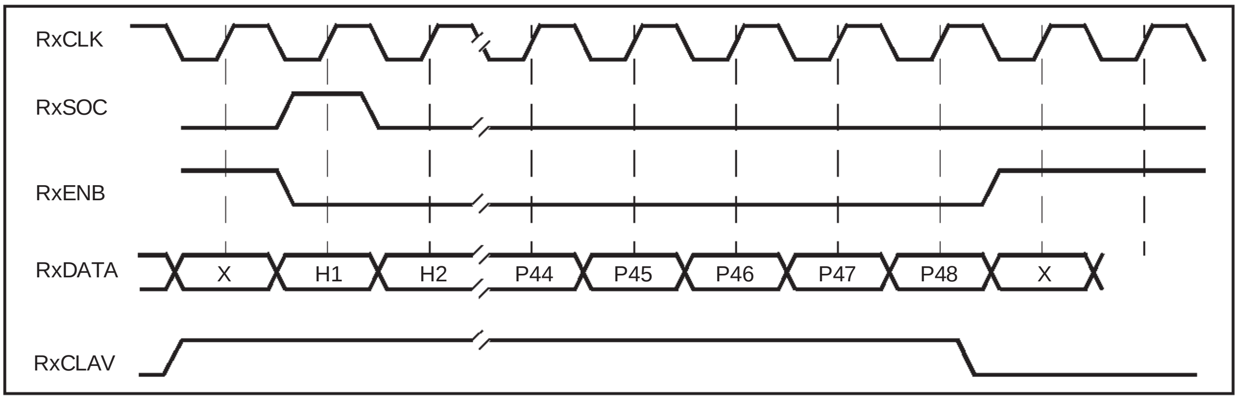
The ATM forum takes the ATM layer chip as a reference. It defines the direction from ATM to physical layer as the Transmit direction.

The direction from physical layer to ATM is the Receive direction. Figures 12 & 13 show the interconnection between ATM and PHY layer devices, the optional signals are not supported and not shown.

The Utopia interface transfers one byte in a single clock cycle, as a result cells are transformed in 53 clock cycles.

Both transmit and receive are synchronized on clocks generated by the ATM layer chip, and no specific relationship between receive and transmit clocks is required. In this mode, the ST70135A can only support one data flow : either interleaved or fast.

Figure 14 : Timing (Utopia 1 Receive Interface)



Pin Description

Name	Type	Meaning	Usage	Remark
RxClav	O	Receive Cell available	Signals to the ATM chip that the ST70135A has a cell ready for transfer	Remains active for the entire cell transfer
RxEnb [1]	I	Receive Enable	Signals to the ST70135A that the ATM chip will sample and accept data during next clock cycle	RxData and RxSOC could be tri-state when RxEnb* is inactive (high). Active low signal
RxClk	I	Receive Byte Clock	Gives the timing signal for the transfer, generated by ATM layer chip.	
RxData	O	Receive Data (8bits)	ATM cell data, from ST70135A chip to ATM chip, byte wide. Rx Data [7] is the MSB.	
RxSOC	O	Receive Start Cell	Identifies the cell boundary on RxData	Indicate to the ATM layer chip that RxData contains the first valid byte of a cell.
RxRef [1]	O	Reference Clock	8 kHz clock transported over the network	Active low signal

Note 1. Active low signal

When RxEnb is asserted, the ST70135A reads data from its internal fifo and presents it on RxData and RxSOC on each low-to-high transition of RxClk, ie the ATM layer chip samples all RxData and RxSOC on the rising edge of RxSOC on the rising edge of RxClk.

Pin Description

Name	Type	Meaning	Usage	Remark
TxClav	O	Transmit Cell available	Signals to the ATM chip that the physical layer chip is ready to accept a complete cell	Remains active for the entire cell transfer
TxEnb [1]	I	Transmit Enable	Signals to the ST70135A that TxData and TxSOC are valid	
TxClk	I	Transmit Byte Clock	Gives the timing signal for the transfer, generated by ATM layer chip.	
TxData	I	Transmit Data (8bits)	ATM cell data, from ATM layer chip to ST70135A, byte wide. TxData [7] is the MSB.	
TxSOC	I	Transmit Start of Cell	Identifies the cell boundary on TxData	TxData contains the first valid byte of the cell.
TxRef [1]	I	Reference Clock	8kHz clock from the ATM layer chip	

Note 1. Active low signal

The ST70135A samples TxData and TxSOC signals on the rising edge of TxClk, if TxEnb is asserted.

TxClk, RxClk, AC Electrical Characteristics

Symbol	Parameters	Min	Max	Unit
F	Clock frequency	1.5	25	MHz
Tc	Clock duty cycle	40	60	%
Tj	Clock peak to peak jitter		5	%
Trf	Clock rise fall time		4	ns
L	Load		100	pF

TxData, TxSOC, AC Electrical Characteristics

Symbol	Parameters	Min	Max	Unit
T5	Input set-up time to TxClk	10		ns
T6	Hold time to TxClk	1		ns
L	Load		100	pF

RxData, RxSOC, RxClav AC Electrical Characteristics

Symbol	Parameters	Min	Max	Unit
T7	Input set-up time to TxClk	10		ns
T8	Hold time to Tx Clk	1		ns
T9	Signal going low impedance to RxClk	10		ns
T10	Signal going High impedance to RxClk	0		ns
T11	Signal going low impedance to RxClk	1		ns
T12	Signal going High impedance to RxClk	1		ns
L	Load		100	pF

Figure 15 : Timing (Utopia 1 Transmit Interface)

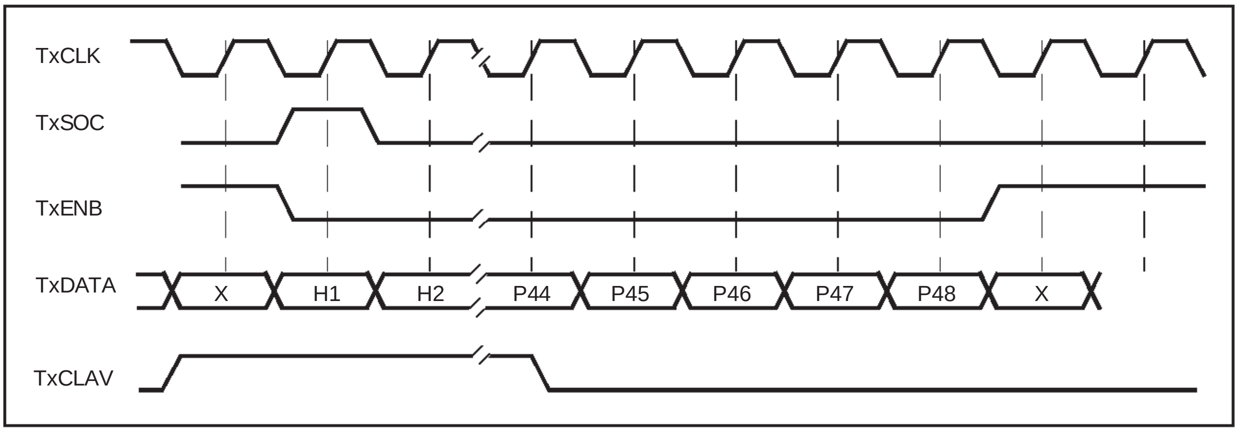
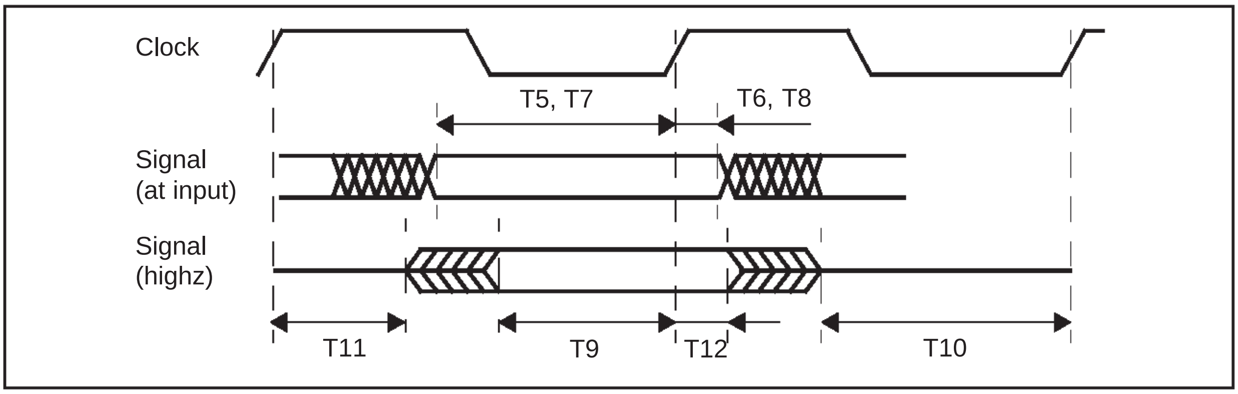


Figure 16 : Timing Specification (Utopia 1)



DIGITAL INTERFACE

Utopia Level 2 Interface

The ATM forum takes the ATM layer chip as a reference. It defines the direction from ATM to physical layer as the Transmit direction. The direction from physical layer to ATM is the Receive direction. Figure 17 shows the interconnection between ATM and PHY layer devices, the optional signals are not supported and not shown.

The UTOPIA interface transfers one byte in a single clock cycle, as a result cells are transferred in 53 clock cycles.Both transmit and receive interfaces are synchronized on clocks generated by the ATM layer chip, and no specific relationship between Receive and Transmit clock is assumed, they must be regarded as mutually asynchronous clocks. Flow control signals are available to match the bandwidth constraints of the physical layer and the ATM layer. The UTOPIA level 2 supports point to multipoint configurations by introducing on addressing capability and by making a distinction between polling and selecting a device:

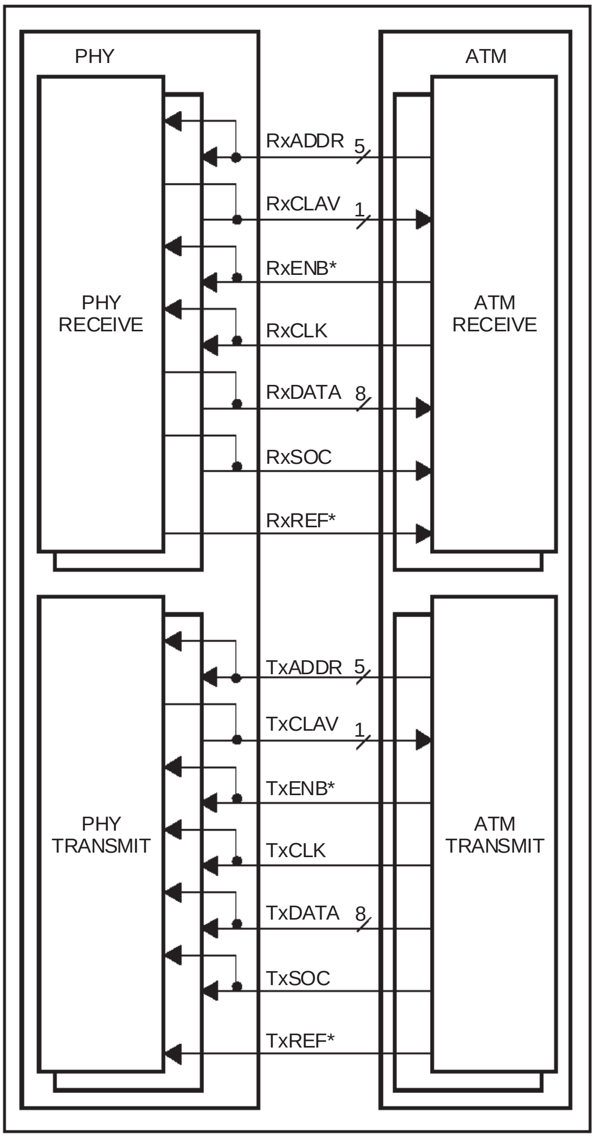
– The ATM chip polls a specific physical layer chip by putting its address on the address bus when the Enb* line is asserted. The addressed physical layer answers the next cycle via the Clav line reflecting its status at that time.
– The ATM chip selects a specific physical layer by putting its address on the address bus when the Enb* line is deasserted and asserting the Enb* line on the next cycle. The addressed physical layer chip will be the target or source of the next cell transfer (see Figure 17).

Utopia Level 2 Signals

The physical chip sends cell data towards the ATM layer chip. The ATM layer chip polls the status of the fifo of the physical layer chip. The cell exchange proceeds like:

a) The physical layer chip signals the availability of a cell by asserting RxClav when polled by the ATM chip.
b) The ATM chips selects a physical layer chip, then starts the transfer by asserting RxEnb*.
c) If the physical layer chip has data to send, it puts them on the RxData line the cycle after it sampled RxEnb* active. It also advances the offset in the cell. If the data transferred is the first byte of a cell, RxSOC is 1b at the time of the data transfer, 0b otherwise.
d) The ATM chip accepts the data when they are available. If RxSOC was 1b during the transfer, it resets its internal offset pointer to the value 1, otherwise it advances the offset in the cell.

Figure 17 : Signal at Utopia Level 2 Interface



ST70135A Utopia Level 2 MPHY Operation

Utopia level 2 MPHY operation can be done by various interface schemes. The ST70135A supports only the required mode, this mode is referred to as ”Operation with 1 TxClav and 1 RxClav”.

PHY Device Identification

The ST70135A holds 2 PHY layer Utopia ports, one is dedicated to the fast data channel, the other one to the interleaved data channel. The associated PHY address is specified by the PHY_ADDR_x fields in the Utopia PHY address register.

Beware that an incorrect address configuration may lead to bus conflicts. A feature is defined to disable (tri-state) all outputs of the Utopia interface. It is enabled by the TRI_STATE_EN bit in the Rx_interface control register.

Pin Description Utopia 2 (Receive Interface)

Name	Type	Meaning	Usage	Remark
RxClav	O	Receive Cell available	Signals to the ATM chip that the STLC60135 has a cell ready for transfer	Remains active for the entire cell transfer
RxEnb*	I	Receive Enable	Signals to the physical layer that the ATM chip will sample and accept data during next clock cycle	RxData and RxSOC could be tri-state when RxEnb* is inactive (high)
RxClk	I	Receive Byte Clock	Gives the timing signal for the transfer, generated by ATM layer chip.	
RxData	O	Receive Data (8 bits)	ATM cell data, from physical layer chip to ATM chip, byte wide.	
RxSOC	O	Receive Start Cell	Identifies the cell boundary on RxData	Indicate to the ATM layer chip that RxData contains the first valid byte of a cell.
RxAddr	I	Receive Address (5 bits)	Use to select the port that will be active or polled	
RxRef *	O	Reference Clock	8kHz clock transported over the network	

*Active low signal

Pin Description Utopia 2 (Transmit interface)

Name	Type	Meaning	Usage	Remark
TxClav	O	Transmit Cell available	Signals to the ATM chip that the physical layer chip is ready to accept a cell	Remains active for the entire cell transfer
TxEnb*	I	Transmit Enable	Signals to the physical layer that TxData and TxSOC are valid	
TxClk	I	Transmit Byte Clock	Gives the timing signal for the transfer, generated by ATM layer chip.	
TxData	I	Transmit Data (8 bits)	ATM cell data, to physical layer chip to ATM chip, byte wide.	
TxSOC	I	Transmit Start of Cell	Identifies the cell boundary on TxData	
TxAddr	I	Transmit Address (5 bits)	Use to select the port that will be active or polled	
TxRef *	I	Reference Clock	8kHz clock from the ATM layer chip	

*Active low signal

BitStream Interface

The Bitstream interface is a proprietary point to point interface. The ST70135A is the bus master of the interface. The interface is synchronous, a common clock is used.

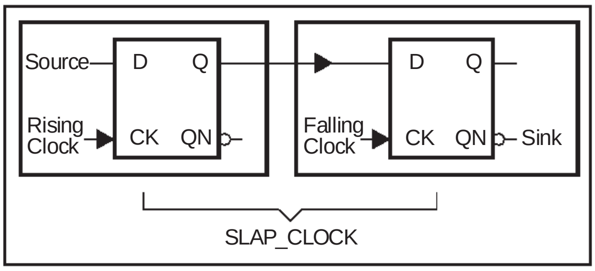
SLAP (Synchronous Link Access Protocol) Interface

The SLAP interface is a point to point bitstream interface. The ST70135A is the bus master of the interface. The interface is synchronous, a common clock (SLAP_CLOCK) is used. The basic idea is illustrated in Figure 17.

The SLAP interface dumps the data of the fast and interleaved channels on 2 separate sub interfaces.

The data flow from the SLAP interface must be enabled by the Transceiver Controller. A disabled cell interface does not dump data on its interface.

Figure 18 : Common Clock Data Transfer



Receive SLAP Interface

The interface signals use 2 signal types: (refer to Figure 19)

– SLR_DATA [1:0]: data pins, a byte is transferred in 4 cycles of 2 bits. The msb are transmitted first, odd bits are asserted on SLR_DATA [1].

– SLR_VAL: indicates the data transfer and the byte boundary

– SLR_FRAME: indicates the start of a super-frame

Notice 2 SLAP interfaces are supported, one for the fast data flow, the other one for the interleaved data flow.

The logic timing diagram is shown in Figure 20.

Figure 19 : Receive Path, SLAP Interface

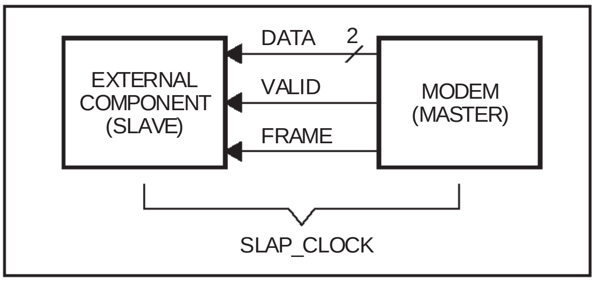
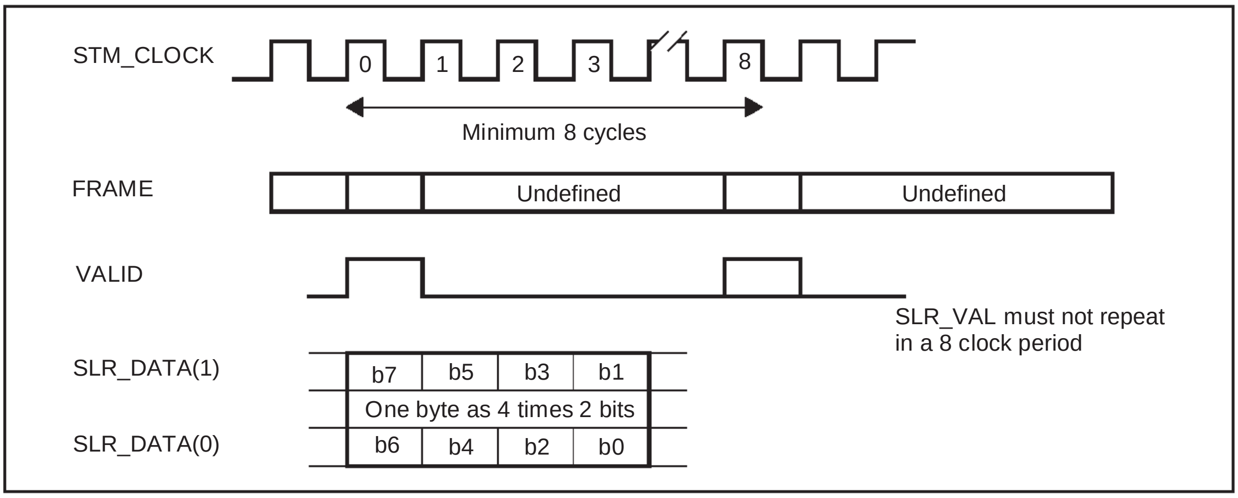


Figure 20 : Receive SLAP Interface Timing



The implementation must guarantee that all active SLR_Valid signals must be separated by at least 8 clock cycles. Refer to Figure 20. The SLR_FRAME signals are asserted when the first pair of bits of a frame are transferred. For the fast channel a frame is defined as a superframe timebase.

For the interleaved channel the frame is defined by a timebase period of 4 superframes. Both timebases are synchronized to the data flow.

Transmit SLAP Interface

The Transmit interface uses the following signals (refer to Figure 21):

– SLT_REQ: byte request.
– SLT_FRAME: start of frame indication.
– SLT_DATA [1:0] data pins, a byte is transferred 2 bits at the time in 4 successive clock cycles. MSB first, odd bits on SLT_DATA [1].

The logical timing diagram is shown in Figure 22. The delay between Request and the associated data byte is defined as 8 cycles.

The SLT_FRAME signals are asserted when the first pair of bits of a frame are transferred. For the fast channel a frame is defined as a superframe timebase.

For the interleaved channel the frame is defined by a timebase period of 4 superframes. Both timebases are synchronized to the data flow and guarantee that the frame indication is asserted when the first bits of the first DMT symbol are transferred.

Figure 21 : Interface Towards PHY Layer

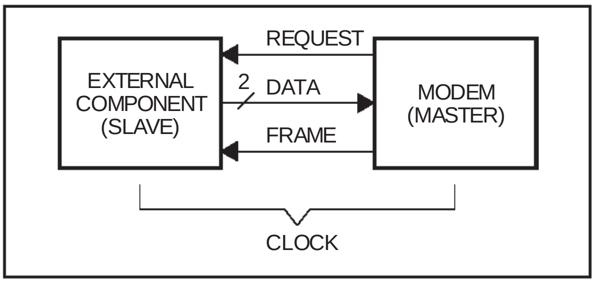


Figure 22 : Interface Timing

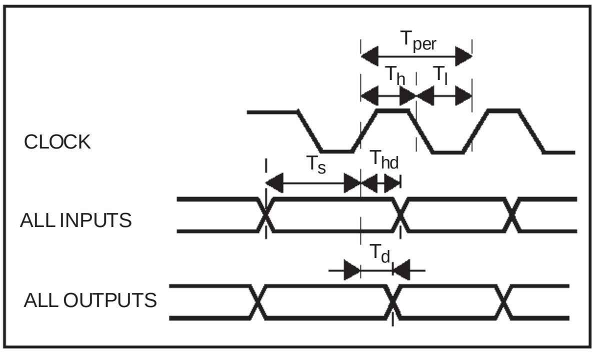
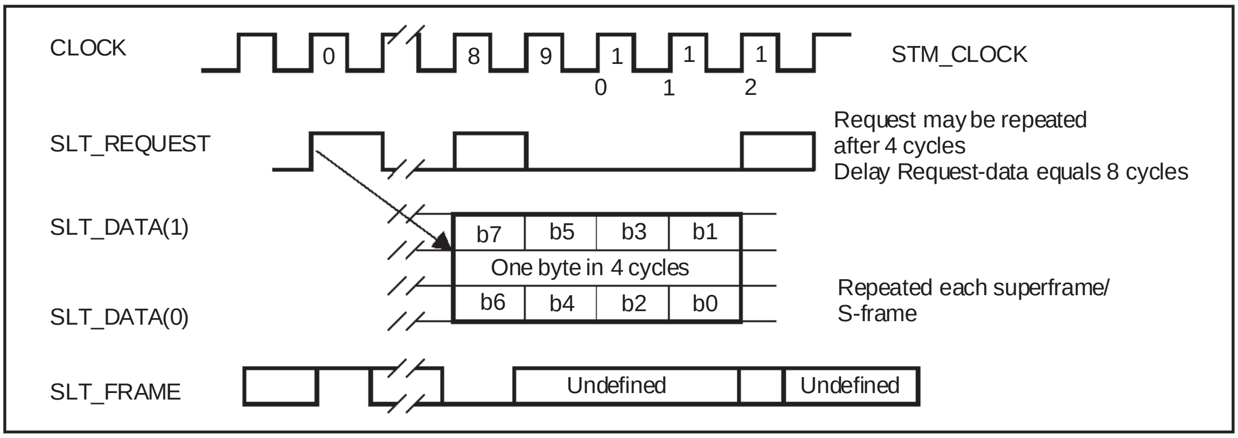


Figure 23 : Transmit SLAP Interface Timing Diagram



SLAP INTERFACE, AC Electrical Characteristics

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
T_{per}	Clock Period	Refer to MCLK				ns
T_h	Clock High		11			ns
T_l	Clock Low		11			ns
T_s	Setup		3			ns
T_{hd}	Hold		2			ns
T_d	Data Delay	20pF load	3		6	ns

Analog Front End Control Interface

The Analog Front End Interface is designed to be connected to the ST70134 Analog Front End component.

Transmit Interface

The 16 bit words are multiplexed on 4 AFTXD output signals. As a result 4 cycles are needed to transfer 1 word. Refer to table 1 for the bit/pin allocation for the 4 cycles.

The first of 4 cycles is identified by the CLWD signal. Refer to Figure 23.

The ST70135A fetches the 16 bit word to be multiplexed on AFTXD from the Tx Digital Front-End module.

Receive Interface

The 16 bit receive word is multiplexed on 4 AFRXD input signals. As a result 4 cycles are needed to transfer 1 word.

Refer to Table 2 for the bit / pin allocation for the 4 cycles. The first of 4 cycles is identified by the CLWD must repeat after 4 MCLK cycles.

Figure 24 : Transmit Word Timing Diagram

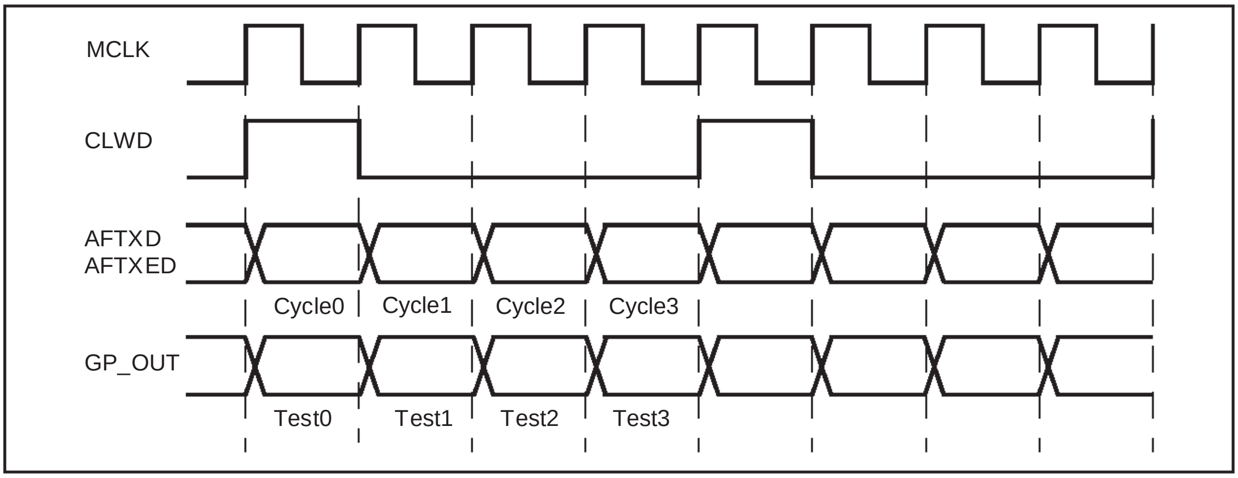


Figure 25 : Receive Word Timing Diagram

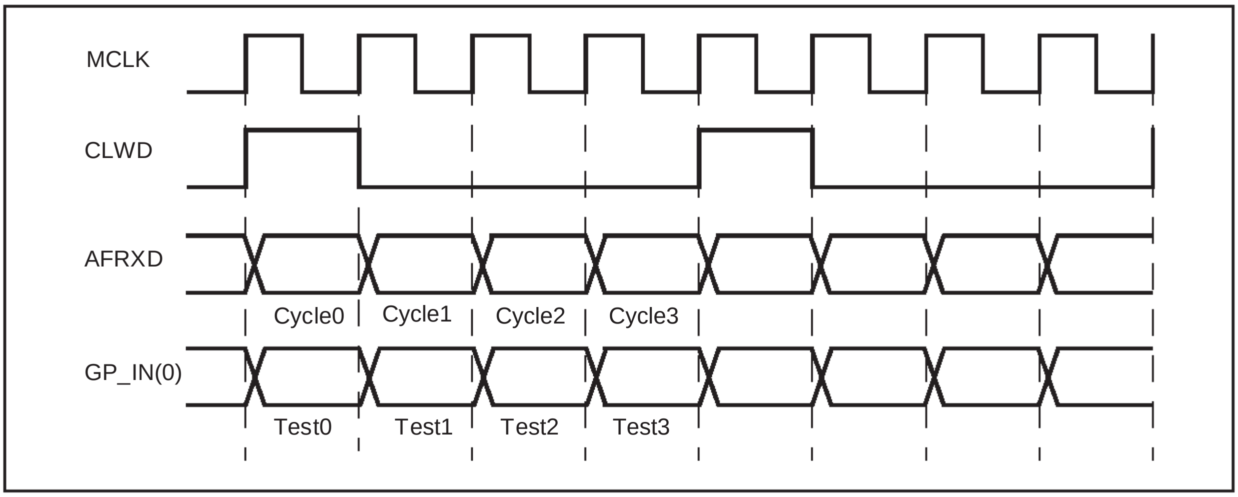


Figure 26 : Transmit Interface

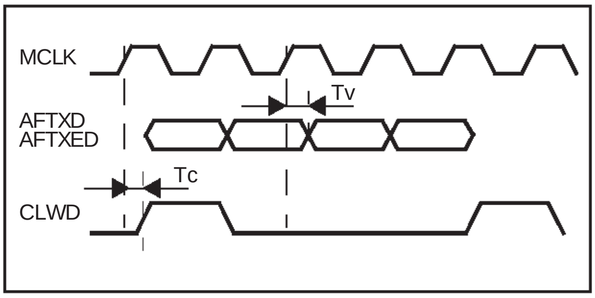


Figure 27 : Receive Interface

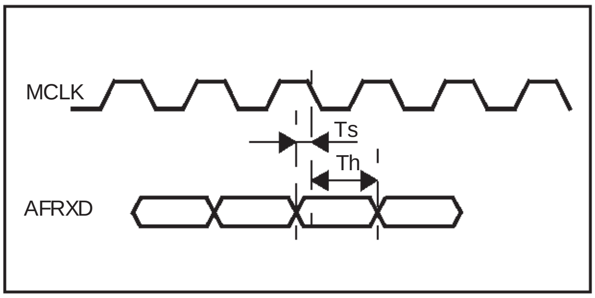


Table 1 : Transmitted Bits Assigned to Signal / Time Slot

	Cycle 0	Cycle 1	Cycle 2	Cycle 3
AFTXD[0]	b0	b4	b8	b12
AFTXD[1]	b1	b5	b9	b13
AFTXD[2]	b2	b6	b10	b14
AFTXD[3]	b3	b7	b11	b15
GP_OUT	t0	t1	t2	t3

Table 2 : Transmitted Bits Assigned to Signal / Time Slot

	Cycle 0	Cycle 1	Cycle 2	Cycle 3
AFRXD[0]	b0	b4	b8	b12
AFRXD[1]	b1	b5	b9	b13
AFRXD[2]	b2	b6	b10	b14
AFRXD[3]	b3	b7	b11	b15
GP_IN	t0	t1	t2	t3

Table 3 : Master Clock (MCLK) AC Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F	Clock Frequency		35.328		MHz
Tper	Clock Period		28.3		ns
Th	Clock Duty Cycle	40		60	%

Table 4 : AFTXD, AFTXED, CLWD AC Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Tv	Data Valid Time	0		10	ns
Tc	Data Valid Time	0		10	ns

Table 5 : AFRXD AC Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Ts	Data setup Time	5			ns
Th	Data hold Time	5			ns

Tests, Clock, JTAG Interface

– Mclk: Master Clock (35.328MHz) generated by VCXO
– ATM receive interface, asynchronous clock generated by Utopia Master
– ATM transmit interface, asynchronous clock generated by Utopia Master
– ATC clock (Pclk): external asynchronous clock (synchronous with ATC in case of i960 specific interface)

JTAG TP interface: Standard Test Access Port, Used with the boundary scan for chip and board testing. This JTAG TAP interface consists in 5 signals:

TDI, TDO, TCK & TMS.

TSRTB: Test Reset, reset the TAP controller. TRSTB is an active low signal.

Table 6 : Boundary Scan Chain Sequence

Sequence Number	Mnemonic	Pin	BS Type
2	AD_0		B
3	AD_1		B
4	AD_2		B
6	AD_3		B
7	AD_4		B
9	AD_5		B
10	AD_6		B
12	AD_7		B
13	AD_8		B
14	AD_9		B
16	AD_10		B
17	AD_11		B
19	AD_12		B
21	PCLK		I
23	AD_13		B
24	AD_14		B
25	AD_15		B
27	BE1		I
28	ALE		C
30	CSB		I
31	WR_RDB		I
32	RDYB		O

Table 6 : Boundary Scan Chain Sequence

Sequence Number	Mnemonic	Pin	BS Type
33	OBC_TYPE		I
34	INTB		O
35	RESETB		I
38	U_RxData_0		B
39	U_RxData_1		B
41	U_RxData_2		B
42	U_RxData_3		B
44	U_RxData_4		B
45	U_RxData_5		B
46	VSS		
47	U_RxData_6		B
48	U_RxData_7		B
50	U_RxADDR_0		I
51	U_RxADDR_1		I
52	U_RxADDR_2		I
53	U_RxADDR_3		I
55	U_RxADDR_4		I
56	GP_IN_0		i
58	GP_IN_1		I
60	U_RxRefB		O
61	U_TxRefB		I
63	U_RxCLK		
64	U_RxSOC		
65	U_RxCLAV		
66	U_RxENBB		
68	U_TxCLK		
69	U_TxSOC		
70	U_TxCLAV		
71	U_TxENBB		
74	U_TxData_7		I
75	U_TxData_6		I
77	U_TxData_5		I
78	U_TxData_4		I
79	U_TxData_3		I
80	U_TxData_2		I
82	U_TxData_1		I

Table 6 : Boundary Scan Chain Sequence

Sequence Number	Mnemonic	Pin	BS Type
83	U_TxData_0		I
84	U_TxADDR_4		I
85	U_TxADDR_3		I
87	U_TxADDR_2		I
88	U_TxADDR_1		I
89	U_TxADDR_0		I
90	SLR_FRAME_F		
92	SLR_FRAME_S		
93	SLR_DATA_S_1		
94	SLR_DATA_S_0		
96	SLR_DATA_S		
97	SLR_DATA_F_1		
98	SLR_DATA_F_0		
99	SLR_VAL_F		
100	SLAP_CLOCK		
101	SLT_FRAME_F		
103	SLT_DATA_F_1		
104	SLT_DATA_F_0		
105	SLT_DATA_S_1		
106	SLT_DATA_S_0		
107	SLT_REQ_F		
110	SLT_REQ_S		
111	SLT_FRAME_S		
112	TDI		
113	TDO		
114	TMS		
116	TCK		
118	TRSTB		
119	TESTSE		none
120	GP_OUT		O
121	PDOWN		O
123	AFRXD_0		I
124	AFRXD_1		I
125	AFRXD_2		I

Table 6 : Boundary Scan Chain Sequence

Sequence Number	Mnemonic	Pin	BS Type
126	AFRXD_3		I
128	CLWD	1	I
129	MCLK	1	C
130	CTRLDATA	1	O
132	AFTXED_0		O
133	AFTXED_1		O
135	AFTXED_2		O
136	AFTXED_3		O
138	IDDq		none
139	AFTXD_0		O
140	AFTXD_1		O
142	AFTXD_2		O
143	AFTXD_3		O

General purpose I/O register

2 general Purpose Register (0x040)

Field	Type	Position Bits	Length	Function
GP_IN	R	[0,1]	2	Sampled level on pins GP_IN
GP_OUT	RW	[2]	1	Output level on pins GP_OUT

Bits from 3 to 15 are reserved

Reset Initialization

The ST70135A supports two reset modes:

– A ’hardware’ reset is activated by the RESETB pin (active low). A hard reset occurs when a low input value is detected at the RESETB input. The low level must be applied for at least 1ms to guarantee a correct reset operation. All clocks and power supplies must be stable for 200ns prior to the rising edge of the RESETB signal.

– ’Soft’ reset activated by the controller write access to a soft reset configuration bit. The reset process takes less than 10000 MCLK clock cycles.

ELECTRICAL SPECIFICATIONS

Generic DC Electrical Characteristics

The values presented in the following table apply for all inputs and/or outputs unless otherwise specified. Specifically they are not influenced by the choice between CMOS or TTL levels. All voltages are referenced to V_{SS}, unless otherwise specified, positive current is towards the device.

IO Buffers Generic DC Characteristics

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
I_{IN}	Input Leakage Current	$V_{IN} = V_{SS}$, V_{DD} no pull up /pull down	-1		1	µA
I_{OZ}	Tristate Leakage Current	$V_{IN} = V_{SS}$, V_{DD} no pull up /pull down	-1		1	µA
I_{PU}	Pull up Current	$V_{IN} = V_{SS}$	-25	-66	-125	mA
I_{PD}	Pull Down Current	$V_{IN} = V_{DD}$	25	66	125	mA
R_{PU}	Pull up Resistance	$V_{IN} = V_{SS}$		50		KΩ
R_{PD}	Pull Down Resistance	$V_{IN} = V_{DD}$		50		KΩ

Input / Output CMOS Generic Characteristics

The values presented in the following table apply for all CMOS inputs and/or outputs unless otherwise specified.

CMOS IO Buffers Generic Characteristics

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{IL}	Low Level Input Voltage				0.2 x V_{DD}	V
V_{IH}	High Level Input Voltage		0.8 x V_{DD}			V
V_{HY}	Schmitt trigger hysteresis	Slow edge < 1V/µs, only for SCHMITx	0.8			V
V_{OL}	Low Level Output Voltage	I_{OUT} = XmA*			0.4	V
V_{OH}	High Level Output Voltage	I_{OUT} = XmA*	0.85 x V_{DD}			V

**Note The reference current is dependent on the exact buffer chosen and is a part of the buffer name. The available values are 2, 4 and 8mA.*

Input/ Output TTL Generic Characteristics

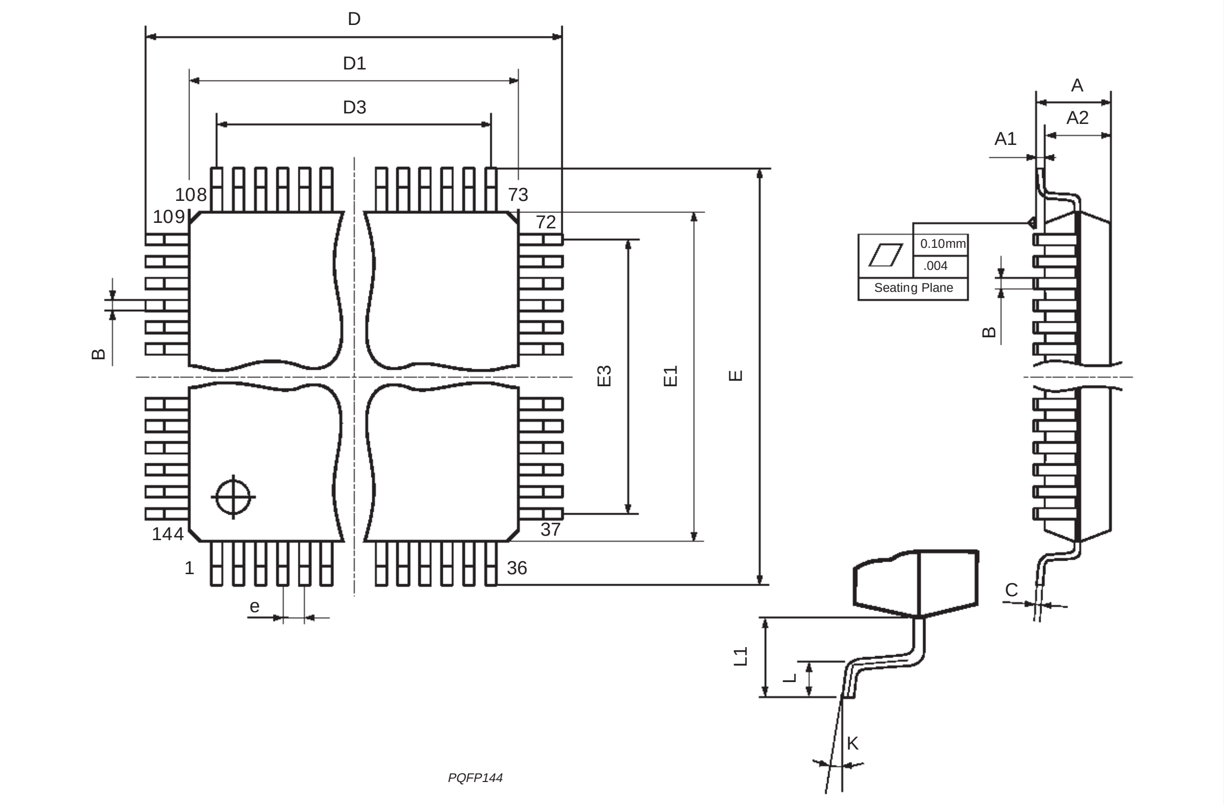
The values presented in the following table apply for all TTL inputs and/or outputs unless otherwise specified.

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{ILHY}	Low Level Threshold, falling	Slow edge < 1V/µs	0.9		1.35	V
V_{IHHY}	High Level Threshold, rising	Slow edge < 1V/µs	1.3		1.9	V
V_{HY}	Schmitt Trigger Hysteresis	Slow edge < 1V/µs	0.4		0.7	V
V_{OL}	Low Level Output Voltage	I_{OUT} = XmA*			0.4	V
V_{OH}	High Level Output Voltage	I_{OUT} = XmA*	2.4			V

**Note The reference current is dependent on the exact buffer chosen and is a part of the buffer name. The available values are 2, 4 and 8mA.*

PQFP144 PACKAGE MECHANICAL DATA

Figure 28 : Package Outline PQFP144



Dimension	Millimeter			Inch		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.144
B	0.22		0.38	0.009		0.015
C	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.219	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		22.75			0.896	
e		0.65			0.026	
E	30.95	31.20	31.45	1.219	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		22.75			0.896	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0° (minimum), 7° (maximum)					